

**REMARKS**

Claims 1-38 are pending in this application. No claims were amended, added or canceled. Claims 1-38 remain in this application.

**Double Patenting Rejection**

Claims 1-38 are rejected under 35 USC 101 as claiming the same invention as that of claims 1-24 of prior U.S. Patent No. 6,606,298.

Pending claim 1 states in part: "scheduling recovery of the 'bad' processor". Claim 1 from U.S. Patent No. 6,606,298 requires: "scheduling recovery of the 'bad' processor *during a predetermined window of time*" as well as an additional limitation "*if the step of attempting recovery takes longer than the window of time, stopping the discovery*". Pending claim 1 does not have these additional limitations, it may be literally infringed without literally infringing claim 1 from U.S. Patent No. 6,606,298. Therefore a statutory double patenting rejection is not appropriate. MPEP 804 (II)(A). Claims 2-6 depend from claim 1 and therefore have the similar ability to be literally infringed without infringing claim 1 of U.S. Patent No. 6,606,298, therefore a statutory double patenting rejection is not appropriate for claims 2-6. MPEP 804 (II)(A).

Pending claim 7 states in part: "one or more modules, each module having a module controller, a memory block and a plurality of digital signal processors for executing code, stored in the memory block, to perform various tasks, the module controller coupled to the plurality of digital signal processors for attempting recovery, during upgrading or recovery, of one or more of the digital signal processors of a particular module having been designated as 'bad'". Claim 7 from U.S. Patent No. 6,606,298 additionally requires: "*the attempted recovery occurring during a predetermined window of time and if the attempted recovery takes longer than the window of time, the module controller for stopping the attempted recovery*".

Pending claim 7 does not have these additional limitations, and may be literally infringed without literally infringing claim 7 from U.S. Patent No. 6,606,298. Therefore a statutory double patenting rejection is not appropriate. MPEP 804 (II)(A). Claims 8-22 depend from claim 7 and therefore have the similar ability to be literally infringed without infringing claim 7 of U.S. Patent No. 6,606,298, therefore a statutory double patenting rejection is not appropriate for claims 8-22. MPEP 804 (II)(A).

Pending claim 23 states in part: "module means including one or more modules, each module having a

module controller, a memory block and a plurality of digital signal processors for executing code, stored in the memory block, to perform various tasks, the module controller coupled to the plurality of digital signal processors for attempting recovery during upgrading or recovery of one or more of the digital signal processors of a particular module having been designated as "bad". Claim 7 from U.S. Patent No. 6,606,298 additionally requires: "*the attempted recovery occurring during a predetermined window of time and if the attempted recovery takes longer than the window of time, the module controller for stopping the attempted recovery*".

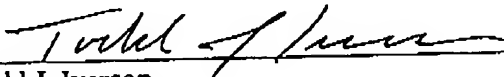
Pending claim 23 does not have these additional limitations, and may be literally infringed without literally infringing claim 7 from U.S. Patent No. 6,606,298. Therefore a statutory double patenting rejection is not appropriate. MPEP 804 (II)(A). Claims 24-38 depend from claim 23 and therefore have the similar ability to be literally infringed without infringing claim 7 of U.S. Patent No. 6,606,298, therefore a statutory double patenting rejection is not appropriate for claims 24-38. MPEP 804 (II)(A).

### CONCLUSION

For the foregoing reasons, reconsideration and allowance of claims 1-38 of the application is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

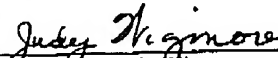
Respectfully submitted,

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I hereby certify that this correspondence  
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(703) 872-9306, on April 25, 2005.

  
Judy Wigmore